being unpatentable over Applicants' Figure 29 in view of Tsukada et al (U.S. Pat. No. 5,266,825).

Firstly, Applicants acknowledge with appreciation the courtesy of Examiner Mandala and Supervisory Patent Examiner Flynn to conduct an interview on this case on December 19, 2002. During the interview, the issues identified in the outstanding Office Action were discussed. Applicants' representative discussed why the combination of Applicants' Figure 29 with Tsukada et al was not obvious. While the examiners indicated that the arguments were reasonable, no decision on patentablility was reached pending further search and/or consideration. Applicant's representative also discussed clarifying changes to Claims 1 and 5 which would make clear that there are first and second parts for both the drain and source regions, such amendments being made solely for the purpose of clarification and not to overcome the applied prior art.

Regarding the objection to Figures 27-29, a Letter Requesting Drawing Change Approval attached herewith shows marked in red a legend --Background Art--. Further, Figure 29 as shown in red deletes reference numeral 39 and the associated arrow, and the specification has been amended to define parasitic capacitance 121. Thus, it is respectfully submitted that the objection to the drawings have been overcome.

Briefly recapitulating, Claim 1 defines a semiconductor device having a silicon on insulator (SOI) substrate including a semiconductor substrate, a dielectric layer, and a semiconductor layer. The semiconductor device includes a transistor having a drain region and source region respectively formed in the semiconductor layer. The drain region has a first part adjacent to the channel region and a second part formed to protrude from the first part of the drain region so that a part of outer peripheries of the drain region extends away

from the gate electrode in a plan view. A first conductor which connects drain wiring to the drain region is connected to the second part of the drain region.

As such, the semiconductor device of Claim 1 addresses, for example, a problem depicted in Applicants' Figure 29 in which parasitic capacitance existing between the source/drain contacts and the gate electrode of the transistor increases as device dimensions are scaled to smaller dimensions. Applicants disclose that:

> ... in accordance with the reduction of the area, the source/drain regions 104, the distance between the contact plugs 103 and the gate 101 becomes smaller, so that parasitic capacitance generated between the two increases, thereby raising a problem of becoming an obstacle against increasing the operation speed and reduction of the electric power consumption.[3]

As illustrated in Applicants' Figure 1, parasitic capacitance can be minimized by contacting to the drain region 2 via the depicted contact plugs 4 in part 3b of the drain region 2 such that the distance between the first conductor and the gate electrode is increased, thereby reducing the parasitic capacitance as compared to a semiconductor device in which the first conductor would be connected to part 3a of the drain region.[4]

As acknowledged in the outstanding Office Action, Applicants' Figure 29 does not disclose a drain region having a second part that protrudes away from a first part and is connected to the drain conductor.[5] The outstanding Office Action, however, asserts that it would have been obvious to combine the teachings of Applicants' Figure 29 with those of Tsukada et al. The Office Action asserts that one skilled in the art would have known that increasing the effective mobility of the transistor would in effect increase defects due to shorts between the gate and the source and/or drain, and that an offset region in the source or

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[3]Specification, page 3, lines 9-13.

[4]Id., page 4, lines 4-8.

[5]Official Action, page 4, line 24 to page 5, line 3.

drain region would increase the area between the source/drain and the gate, which would decrease the chances of shorts or parasitic capacitances.[6] Applicants respectfully disagree with the first part of this assertion which relates to the chances of shorts, and point out that the other part of this assertion which relates to decreasing parasitic capacitance is derived only from Applicants' disclosure and not from the applied art.

Regarding the chance of shorts, an offset region in the source or drain region would not decrease the chances of shorts. For example, the continued existence of the region shown in Applicants' Figure 28 between the source/drain regions 104 means that the chances of an electrical short is not decreased despite having added an offset region such as that shown as part 3b in Applicants' Figure 1. To decrease the chances of an electrical short, the width of the channel region would have to be increased along with an increased separation of the gate electrode from the source/drain regions.

Furthermore, a drain region formed in the semiconductor layer defined in Claim 1 has an offset (i.e., a second part formed to protrude from the first part of the drain region so that a part of outer peripheries of the second part of the drain region extends away from the gate electrode in a plan view), whereas in Tsukada et al the drain electrode 9 is formed on the silicon substrate and has an offset as shown in Figures 1(a) and 1(b) of Tsukada et al which as shown in Figure 1(a) extends along a direction of the gate electrode, see for example the extension of the gate electrode 2 in Tsukada et al depicted at the bottom of Figure 1(a). Accordingly, the drain electrodes of Claim 1 and of Tsukada et al are explicitly different from each other in structure, with there existing in Tsukada et al parasitic capacitance to the gate

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[6]Office Action, page 5, lines 3-8.

electrode 2 which is not alleviated by the offset of the contact 11 from the drain region 9 in Tsukada et al.

Regarding decreasing the parasitic capacitance to the gate electrode, Applicants respectfully submit that only in Applicants' disclosure, and not in Tsukada et al, is there proper motivation for adding an offset region to a silicon-on-insulator (SOI) device. First of all, Tsukada et al is silent as to the purpose of the offsets to the drain and source regions shown in Figure 1(a). More importantly, Tsukada et al, in addressing problems associated with scaling down the dimensions of an amorphous silicon thin film device used to drive display devices, address a different problem by using a different solution than that addressed by Applicants' invention in scaling down the dimensions of a SOI device. Indeed, the solution taught by Tsukada et al, in ***adding capacitance*** to the gate electrode, teaches away from the present invention which minimizes capacitance to the gate electrode. Tsukada et al disclose that:

> ... The above previous application makes it possible to effectively increase the mobility of the thin-film transistor by three to five times while permitting the transistor to exhibit improved reliability. In the above previous application, however, the thickness of the insulating film must be decreased between the second gate electrode and the channel region, still giving rise to the occurrence of defects due to shorts between the gate and the source or between the gate and the drain. Therefore, there is little design margin or process margin, and problem arises when the elements are applied in an integrated form to the active matrix liquid crystal display and the like.
>
> According to the present invention, ***a coupling capacity is connected*** in series ***with the gate electrode*** of a thin-film transistor as a unitary structure, and a bias voltage is applied to the electrode via the coupling capacity.
>
> In order to improve the yield of transistors, in this case, ***the coupling capacity is formed*** outside the channel region of the transistor as viewed or a plane. This constitution is effective particularly when the transistors are arrayed.[7] [emphasis added]

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[7]Tsukada et al, column 1, line 58, to column 2, line 12.

Thus, to improve the yield of amorphous silicon devices driving liquid crystal displays, Tsukada et al disclose the addition of capacitance (i.e. capacity 12 shown in Figure 1(a)) to the gate electrode.

Indeed, a large junction capacitance is formed across a channel in the structures shown in Figures 1(a) and 1(b) of Tsukada et al in which an N^+ layer 5 is formed on an amorphous silicon layer 4, resulting in a decrease in operation speed of a transistor. In this respect, Applicants submit that the junction capacitance in the device of Tsukada et al could be reduced by approximately a factor of 10 by the semiconductor device of claim 1 in which a drain region and a source region are formed in a semiconductor layer of an SOI substrate.

Adding capacitance to a gate electrode of a SOI device, as discussed previously in reference to Applicants' Figure 1, is exactly ***the opposite*** of that needed to increase the operational speed and electrical losses in SOI devices. Thus, the teachings of Tsukada et al, when taken as a whole, ***teach away*** from the present invention and provide no reasonable expectation of success in that the additional capacitance would frustrate operation of a SOI device which by its silicon isolation on an insulator seeks to minimize various parasitic capacitances.

Thus, except for Applicants' specification, there exists no teaching or suggestion for the SOI semiconductor device defined in Claim 1. M.P.E.P. §2143 states that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not applicant's disclosure.

Hence, with no teaching or suggestion in Tsukada et al for minimizing capacitance to the gate electrode, there exists no proper suggestion or motivation for one of ordinary skill in the art to combine the features shown in the amorphous silicon transistor of Tsukada et al with

Applicants' SOI device in Figure 29. Hence, Claim 1 and Claims 2 and 5-6 which depend from Claim 1 are believed to patentably define over the applied prior art.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE SPECIFICATION

Please amend the paragraph on page 3, beginning at line 9, as shown below:

However, in accordance with the reduction of the area of the source/drain regions 104, the distance between the contact plugs 103 and the gate electrode 101 becomes smaller, so that parasitic capacitance 121 generated between the two increases, thereby raising a problem of becoming an obstacle against increase of the operational speed and reduction of the electric power consumption.

IN THE CLAIMS

Please amend the claims as shown below:

1. (Amended) A semiconductor device comprising:

an SOI substrate having respectively a semiconductor substrate, a dielectric layer, and a semiconductor layer [formed in this order];

a transistor having a drain region and a source region respectively formed in said semiconductor layer[, and];

a gate electrode formed via a gate dielectric film on a channel region sandwiched between said drain region and said source region;

an interlayer dielectric film formed on said transistor;

a drain wiring and a source wiring formed on said interlayer dielectric film;

a first conductor formed in said interlayer dielectric film [for] and connecting said drain wiring to said drain region; [and]

a second conductor formed in said interlayer dielectric film [for] and connecting said source wiring to said source region[, wherein];

said drain region [has] including,

a first part [being] adjacent to said channel region, and

a second part formed to protrude from said first part of the drain region so that a part of outer peripheries of said second part of said drain region extends away from said gate electrode in a plan view[,]; and

said first conductor is connected to said second part of said drain region.

5. (Amended) The semiconductor device according to claim 1, wherein said source region [has] comprises:

a first part [being] adjacent to said channel region; and

a second part formed to protrude from said first part of the source region so that a part of outer peripheries of said second part of said source region extends away from said gate electrode in a plan view, [and] said second conductor [is] connected to said second part of said source region.